REMARKS

At the time the current Official Action was mailed, claims 32-91 were pending in the above-identified application. In the Official Action, the Examiner objected to claims 37, 40, 52, 55, 67, 70, 82, and 85, and rejected claims 32-36, 38, 39, 41-51, 53, 54, 56-66, 68, 69, 71-81, 83, 84 and 86-91. By this present Response, the title and claims 32 and 47 have been amended. Claims 32-91 remain pending. Reconsideration and allowance of all pending claims are requested.

Objections to the Specification

The Examiner objected to the title as not being clearly indicative of the invention to which the claims are directed. Accordingly, Applicants have amended the title. Applicants respectfully submit that the new title is sufficiently indicative of the invention as presently claimed, and Applicants respectfully request withdrawal of the Examiner's objection.

Rejections under 35 U.S.C. § 102

The Examiner rejected claims 32-33, 38-39, 41-48, 53-54, 56-63, 68-69, 71-78, 83-84 and 86-91 under 35 U.S.C. § 102(e) as being anticipated by Klersy et al. (U.S. Patent No. 5,536,947). Specifically, the Examiner stated:

> Klersy et al. discloses the claimed memory cell (Figs. 1 and 2) comprising an area defined by an intersection of a word line 42 and a bit line 12; an access device (32, 34); a memory element operatively coupled to the access device, the memory element comprising dielectric material 46 having a pore therein; a first electrode 48 disposed within the pore; a memory material 36 disposed over the first electrode a second electrode (38, 40) disposed over the memory material; and wherein the access device and the memory element are disposed wholly in the area. The current photolithographic limit is about 0.2um. Klersy et al. discloses a memory cell wherein the pore diameter is as low as

0.01 um (col. 17, lines 20-23). Therefore, the pore is smaller than the photolithographic limit.

Regarding claims 33, 48, 63 and 78, the access device comprises a diode 26 (Fig. 3).

Regarding claims 38, 53, 68, and 83, the second electrode comprises a plurality of layers (38, 40).

Regarding claims 39, 54, 69, and 84, the second electrode comprises a plurality of materials.

Regarding claims 41-46, 56-61, 71-76 and 86-91, the memory material 36 comprises structure changing material of a chalcogenide material which inherently changes between different states of crystallinity in response to electrical stimulus, wherein each of the different states of crystallinity corresponds to a given resistance level. The chalcogenide material comprises a programmable resistive element that changes between different resistance levels in response to electrical stimulus.

Regarding claims 62 and 77, Klersy et al. further discloses a first conductive line 12 extending in a first direction; a second conductive line 42 extending in a second direction different that the first direction, the first conductive line and the second conductive line being spaced apart by a portion of a substrate, the second conductive line intersecting the first conductive line in an overlapping manner to form an area of intersection in the portion of the substrate, the access device (diode) being operatively coupled to the first conductive line, the memory element wholly disposed in the area of intersection.

Prior to addressing this rejection, Applicants would like to remind the Examiner that "the Examiner should never overlook the importance of his or her role in allowing claims which properly define the invention." M.P.E.P. § 706. Applicants would further like to remind the Examiner that the "goal of examination is to clearly articulate any rejection early in the prosecution process so that the Applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity." *Id.* In the present application, Applicants respectfully, but firmly, believe that the Examiner has lost sight of these two very

important goals. The Examiner applied the Klersy reference nearly *two years* ago in the Official Action mailed on November 27, 2001. In the Response filed by Applicants on February 27, 2002, Applicants effectively described several reasons why the Klersy reference did not disclose the claimed subject matter. Subsequently, in the Official Action mailed on November 19, 2002, the Examiner did not reject any of the claims based upon prior art although the Klersy reference was certainly still available to the Examiner. Instead, the Examiner merely rejected claims 32-91 under 35 U.S.C. § 112, first paragraph, and Applicants obviated this rejection by correcting a clear error in Figs. 4-15. The Examiner did not reject the claims under 35 U.S.C. § 112, second paragraph, as being indefinite, nor did the Examiner state that the claims were difficult to understand for any other reason. Therefore, if the Examiner believed that any of the cited prior art rendered the claimed subject matter unpatentable, appropriate rejections should have been set forth at that time.

In view of the fact that Applicants had previously overcome the prior art cited by the Examiner, and further in view of the fact that the Examiner did not provide a prior art rejection in a more timely manner, prosecution of the present application has been unduly and unnecessarily prolonged. Indeed, in view of the remarks set forth above and below, Applicants respectfully submit that the claimed subject matter is patentable over the prior art of record and respectfully requests immediate allowance of claims 32-91. If the Examiner chooses not to allow claims 32-91 in view of the remarks set forth herein, Applicants respectfully request a telephonic interview with the Examiner and the Examiner's supervisor prior to the issuance of another Official Action.

Applicants respectfully traverse this rejection. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

In regard to the present rejection, as set forth in Applicants' Response mailed on February 27, 2002, the Klersy reference discloses nothing more than a prior art memory cell, such as that described in the present application on Page 5, lines 7-23. The memory cell disclosed in the Klersy reference exhibits many of the disadvantages that the present techniques address. Specifically, the Klersy memory cell is inoperative until the dielectric layer 48 is "popped" by a current that is much higher than the current required to program or read the memory cell. The Klersy reference clearly supports this assertion by stating that higher current pulses must be delivered to the newly constructed memory element until the layer 48 breaks down, after which lower current electrical cycling can take place for programming and reading. *See Klersy*, col. 17, line 56, to col 18, line 17. In contrast, Applicants have devised a memory cell in which high current through the access device is not needed, so that the access device *and* the memory cell can be made small enough to be disposed wholly within the intersection of a word line and a bit line, thus creating an X-point memory cell.

The Examiner is correct that the Klersy reference does disclose a diode 26 to be used as an access device as illustrated in Fig. 3. However, the Examiner's rejection fails for several reasons. Although Fig. 3 clearly shows an access diode 26 coupled to a memory cell 30, it is equally clear that Fig. 1 does not illustrate the access diode 26--it merely illustrates the memory cell 30. The Examiner has stated that the access diode 26 includes layers 32 and 34, as set forth in Fig. 1, but this assertion is clearly erroneous. The Klersy reference repeatedly refers to elements 6 and 8 as "contacts" that are disposed on either side of the memory material 36 and that are clearly part of the memory cell 30. The Klersy reference further discloses that the contact 8 includes elements 32 and 34. Element 34 is a diffusion barrier layer that inhibits the migration of foreign material into the memory material 36, and element 32 is a thin film of metal, such as titanium and/or tungsten, having excellent ohmic contact properties, as well as barrier properties. *See* col. 14, line 55, to col. 15, line 24; col. 15, lines 37-55. Because the two layers 32 and 34 clearly form one of the contacts 8 of the memory cell 30, and clearly do not form the diode 26, the Examiner' s assertion to the contrary is clearly in error and not supported in any manner by the Klersy reference.

Based on the remarks set forth above, it is clear that the Klersy reference does not specifically disclose an access device sized such that it is disposed wholly in an area defined by an intersection of a word line and a bit line, as set forth in the present claims. Moreover, Applicants respectfully submit that the Klersy reference does not inherently disclose such an access device either. Indeed, the access diode 26 undoubtedly would be formed in the substrate 10, and the size of the access diode 26 certainly would be wider than other portions of the memory cell 30 due to the very high currents that it must carry to break down the dielectric layer 48. As discussed in the present application, it is crucial to reduce the current-carrying duties of

the access device to produce a smaller memory cell. The way to reduce the size of the access device is to reduce the amount of current it must carry. Since any memory cell that uses "popping" to form a path through the chalcogenide material requires even higher current, any such memory cell must be considered as teaching away from the present technique.

In view of the remarks set forth above, Applicants respectfully submit that the subject matter of the rejected claims is patentable over the Klersy reference. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of the rejected claims.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 34, 49, 64, and 79 under 35 U.S.C. § 103(a) as being unpatentable over Klersy et al. (U.S. Patent No. 5,536,947) as applied to claims 32, 47, 62, and 77 above, and further in view of Wang et al. (U. S. Patent No. 4,616,404). Specifically, the Examiner stated:

> Klersy et al. as described above does not disclose the diode 26 comprising a layer of N doped polysilicon disposed adjacent a later of P doped polysilicon. It is old and well known in the art that a diode is routinely formed of a layer of N doped polysilicon and a layer of P doped polysilicon as shown for example by Wang et al. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the diode 26 of Klersy et al. comprising a layer of N doped polysilicon and a layer of P doped polysilicon to form a polysilicon diode with low reverse current leakage and low series reisistance permitting high current flow.

Furthermore, the Examiner rejected claims 35-36, 50-51, 65-66, and 80-81 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Klersy et al. (U. S. Patent No. 5,536,947) as applied to claims 32, 47, and 62 above, and further in view of Ovshinsky et al. (U. S. Patent No. 5,414,271). Specifically, the Examiner stated:

> Klersy et al. as described above does not disclose the first electrode 48 comprising a plurality of layers and a plurality of materials. Ovshinsky et al. discloses the first electrode comprising two layers (32 and 34) of different of materials (carbon and molybdenum). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the first electrode 48 of Klersy comprising two layers of the materials as taught by Ovshinsky et al. in order to form excellent electrical contacts with the memory material 36.

Applicants respectfully traverse these rejections. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the

obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

As discussed at length above, the Klersy reference does not illustrate or otherwise disclose that the access diode 26 is sized and disposed relative to the memory cell 30 such that the Klersy reference discloses an X-point memory cell. In regard to the Examiner's Section 103 rejection based on a combination of the Klersy and Wang references, it seems that the Examiner has at least partially recognized the deficiency of the Klersy reference due to the Examiner's mistaken belief that layers 34 and 32 constitute the access device 26 instead of the electrical contact 8. However, any attempt to utilize the Wang reference to overcome this "deficiency" is nonsensical. As discussed above, the access device 26 is not disclosed in Figure 1 of the Klersy reference, and the layers 32 and 34 clearly form a contact 8 of the memory cell 30 –not an access diode 26 as asserted by the Examiner. Furthermore, it is equally clear that the layers 32 and 34 could not possibly function as any sort of a diode. Therefore, there would be no suggestion whatsoever to replace the electrical contact 8 with a P-N junction diode of Wang. Consequently, the Examiner's rejection based on a combination of the Klersy and Wang references must fail.

Similarly, the Examiner's Section 103 based on a combination of the Klersy and Ovshinksy references also fails due to the Examiner's gross misinterpretation of the Klersy disclosure. Specifically, the Examiner has attempted to classify element 48 of the Klersy reference as an "electrode." Presumably, the Examiner misclassified element 48 as an electrode so that the Examiner could misclassify elements 34 and 32 as a diode. However, the Klersy reference clearly teaches that element 48 is a "filament confining means" that is

disposed between at least one of the contacts 8 and the memory material 36. Klersy, col. 17, lines 24-55. The Klersy reference further teaches that the filament confining means 48 is a dielectric material that is "popped" to form the memory pore. Klersy, col. 17, line 56, to col. 18, line 18. Because element 48 of the Klersy reference is clearly a dielectric through which pores of memory material are formed, rather than an electrical contact, there is no suggestion to modify element 48 to use a plurality of layers of electrode material, such as carbon and molybdenum, as set forth in the Ovshinksy reference. Accordingly, this rejection must also fail.

In view of the remarks set forth above, Applicants respectfully submit that the rejected claims are patentable over the cited combinations. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of the rejected claims.

General Authorization for Fee Payments and Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, **Applicants authorize the Commissioner to charge the fee for the two-month extension of time to the credit card listed on the attached PTO FORM 2038**. However, if the fees cannot be charged as indicated for any reason, Applicants authorize the Commissioner to charge any additional fees which may be required, to Deposit Account No. 13-3092; Order No. MCRO:0106-2/FLE (95-0412.02).

Respectfully submitted,

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